REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-8 and 15 stand rejected under 35 U.S.C. §103(a) as unpatentable over Chen in view of Wang and Lee.

Having carefully considered the references, the applicants disagree with the examiner's conclusions, particularly as to the secondary references. With the understanding that Chen is similar to the present invention in the sense that they are each directed to the fabrication of a semiconductor substrate by practicing the steps of forming an oxide film over a semiconductor substrate (followed by other steps), Lee is relied upon to supply the teaching of a rapid thermal annealing step.

Under the examiner's analysis of the teachings of the references and the differences between same and the claimed invention, it is indicated that Lee teaches a rapid thermal annealing step to minimize transient enhanced diffusion of halo dopants during the preparation of a semiconductor. However, this is in substantial contrast to the claimed invention, as Lee does not teach or suggest rapid thermal annealing of the oxide film **after** it has been applied to the semiconductor substrate. Accordingly, the person of skill in the art would recognize that, not only are there are substantial differences between the combination of prior art and claimed invention, but that the combined prior art **teaches away** from the claimed invention. The RTA step of Lee is performed during the fabrication of the semiconductor, or in other words, RTA would take the place at a time prior to application of the oxide film.

Claims 16-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chen in view of Wang (US 6,448,167).

Wang suggests a method including forming a RPO (resistor protect oxide) layer, carrying out RTA, and removing the RPO layer. Thus, the combination of Chen and Wang teaches a method including the steps of:

(a) forming STI;

(b) carrying out ion implantation;

(c) forming a RPO layer;

(d) carrying out RTA;

(e) removing the RPO layer;

(f) forming an electrically insulating film;

(g) removing the electrically insulating film;

(h) forming a metal film; and

(i) carrying out second annealing.

In the method defined in claim 16, the oxide film formed in the step (c) subsequent to the implantation of impurity ions provides a silicide block in the non-silicide transistor region that is mentioned in Claim 16 part (e).

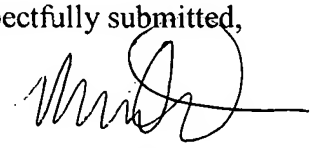
According to the combination of Chen in view of Wang that is discussed above, using the oxide film as a silicide block is not disclosed or suggested by the combined teachings. Moreover, rapid thermal annealing will occur between steps (b) and (c). This is in contrast to the invention recited in claim 16, in which no thermal-annealing step is carried out between said (b) and (c), so as to prevent a recess at a shoulder of said shallow trench isolation film from deepening.

Also, since the method provided by the combination of Chen and Wang includes two steps of removing an insulating film, that is, the steps (e) and (g), the combination cannot prevent a recess to be formed at a shoulder of a STI film from becoming deep. This is in contrast to the

present invention.

Wherefore, based upon the foregoing, it is respectfully submitted that the present application is in condition of allowance and a relatively early reply is requested.

Respectfully submitted,



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